9. (Twice Amended) A ferroelectric memory device comprising:

a ferroelectric capacitor including a top electrode, a bottom electrode and a ferroelectric film interposed between the top and bottom electrodes, the top electrode having a rectangular planar pattern;

a memory cell transistor including first and second doped layers and a gate, the memory cell transistor controlling a voltage supplied to the top electrode of the ferroelectric capacitor;

an interlevel dielectric film formed over the memory cell transistor and the ferroelectric capacitor;

a first interconnection layer formed on the interlevel dielectric film;

an upper interlevel dielectric film formed to cover the first interconnection layer; and

a second interconnection layer formed on the upper interlevel dielectric film, wherein, in a planar layout of the ferroelectric memory device, the first interconnection layer partially overlaps with the top electrode of the ferroelectric capacitor, and does not cover at least one side of the rectangular top electrode, and the width of a bit line formed above the top electrode is smaller than the distance between the top electrode and another top electrode adjacent to the top electrode.

REMARKS

At the outset, the Examiner is thanked for the review and consideration of the present application.

The Examiner's Office Action dated February 13, 2002, has been received and its contents reviewed. By this Amendment claims 1, 6, 8, and 9 have been amended. Accordingly, claims 1-11 are pending in the present application, of which claims 1 and 9 are independent.

Turning now to the Office Action, the drawing are objected to as failing to show every feature of claim 8 and 9. Further, the specification is objected under 37 C.F.R 1.71 as failing to provide adequate written description for the features in claims 8 and 9. In response, Applicants have amended claims 8 and 9, as shown above. Accordingly, the objections are respectfully requested to be reconsidered and withdrawn.

Claims 1-7, and 8 are rejected under 35 U.S.C. §112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time of the application was filed, had possession of the claimed invention. More specifically, claim 1 recites "dummy bit lines..." which is not described in the specification, and claim 8 recites "the upper interlevel" which lacks proper antecedent basis. In response, Applicants have amended claims 1 and 8, as shown above, to overcome the rejection. Accordingly, the §112, first paragraph, rejection of claims 1-7, and 8 is respectfully requested to be reconsidered and withdrawn.

Claims 1-7 are rejected under 35 U.S.C. §103(a) as unpatentable over Applicant Admitted Prior Art (AAPA) in view of Chinu et al. (JP 11-121705A - hereafter Chinu), and claims 8-10 are rejected under 35 U.S.C. §103(a) as unpatentable over Chinu in view of Hayashi et al. (U.S. Patent No. 6,174,766 - hereafter Hayashi). These rejections are respectfully traversed at least for the reasons provided below.

Chinu teaches that the first interconnection extends in two directions of left and right, with respect to the vertical extension of the bottom electrode. Moreover, a plurality of the top electrodes is arranged in two parallel rows with respect to the direction of the extension of the bottom electrode.

Hence, in Chinu, since the first interconnection extends in two directions of left end right, with respect to the vertical extension of the bottom electrode, the tensile stress of the first interconnection is applied on the bottom electrode in the same directions. As a result, stress is applied on the dielectric film and the degrading of the capacitor occurs.

However, according to the amended claim 1 of the present invention, the first interconnection, which connects to the plurality of the top electrodes , extends in only one direction of left or right with respect to the vertical extension of the bottom electrode. Moreover, since tensile stress of the first interconnection layer is not applied to the bottom electrode, stress is not applied on the dielectric film and the degrading of the capacitor can be prevented.

Further, the object of Chinu is to integrate memory, which is different from that of the present invention of reducing stress on dielectric film. Moreover, in Chinu, if plurality of top electrodes is arranged in a row on top of one bottom electrode as in the present invention, separations between adjacent bottom electrodes are required, thus preventing surface integration,

which would be teaching away from the object of Chinu.

Further, since the object of Chinu is to integrate memory and not to reduce stress on dielectric film, the combination of Chinu and the prior art would be difficult without proper suggestion or motivation. Even if the combination were possible, the combination would teach away from the object of Chinu as shown above.

Moreover, the object of Chinu is different from that of the present invention, and Chinu does not teach, disclose, or suggest all of the features of Applicants' independent claim 1 and its dependent claims, the application of Chinu, combined with other cited prior art or applied separately, would be improper.

In view of the arguments and amendments set forth above, Applicants respectfully request reconsideration and withdrawal of all the §103(a) rejections of claims 1-11.

CONCLUSION

Having responded to all rejections set forth in the outstanding non-Final Office Action, it is submitted that claims 1-11 are now in condition for allowance. An early and favorable Notice of Allowance is respectfully solicited. In the event that the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of the above claims, the Examiner is courteously requested to contact Applicants' undersigned representative.

Respectfully submitted,

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MARKED-UP VERSION OF AMENDED CLAIMS

1. (Four Times Amended) A ferroelectric memory device comprising:

a ferroelectric capacitor including a top electrode, a bottom electrode and a ferroelectric film interposed between the top and bottom electrodes, the top electrode having a rectangular planar pattern;

a memory cell transistor including first and second doped layers and a gate, the memory cell transistor controlling a voltage supplied to the top electrode of the ferroelectric capacitor;

[an] a first interlevel dielectric film formed over the memory cell transistor and the ferroelectric capacitor;

a first interconnection layer formed on the first interlevel dielectric film; and

a memory cell composed of the ferroelectric capacitor and the memory cell transistor[; and

dummy bit lines connected to the ferroelectric capacitor that is not used for the circuit operation],

wherein, in a planar layout of the ferroelectric memory device, the first interconnection layer partially overlaps with the top electrode of the ferroelectric capacitor, and does not cover at least one side of the rectangular top electrode, and the width of a bit line formed above the top electrode is smaller than the distance between the top electrode and another top electrode adjacent to the top electrode;

wherein the memory cell comprises a memory cell array arranged in a matrix, [and

wherein the dummy bit line is arranged at the edge of the memory cell array] wherein the first interconnection layer extends only in one direction with respect to the top and bottom electrodes, and

wherein a plurality of the top electrode is arranged only in a row with respect to the direction of the length of the bottom electrode.

6. (Amended) The device of Claim 1, wherein the first interconnection layer includes:

a storage line connected to the top electrode of the ferroelectric capacitor and to the first doped layer of the memory cell transistor, the storage line having a linear planar pattern; and

[a] the bit line connected to the second doped layer of the memory cell transistor, and wherein the bit line does not overlap with the top electrode in the planar layout.

8. (Twice Amended) [A ferroelectric memory device comprising:

a ferroelectric capacitor including a top electrode, a bottom electrode and a ferroelectric film interposed between the top and bottom electrodes, the top electrode having a rectangular planar pattern;

a memory cell transistor including first and second doped layers and a gate, the memory cell transistor controlling a voltage supplied to the top electrode of the ferroelectric capacitor;

an interlevel dielectric film formed over the memory cell transistor and the ferroelectric capacitor;

a first interconnection layer formed on the interlevel dielectric film;

a second inteconnection layer formed on the upper interlevel dielectric film,]

The device of Claim 1 further comprising:

a second interlevel dielectric film formed to cover the first interconnection layer,

wherein, in a planar layout of the ferroelectric memory device, the first interconnection layer partially overlaps with the top electrode of the ferroelectric capacitor, and does not cover at least one side of the rectangular top electrode, and the width of a bit line formed above the top electrode is smaller than the distance between the top electrode and another top electrode adjacent to the top electrode[; and

wherein the second interconnection layer totally covers the top electrode of the ferroelectric capacitor in the planar layout].

9. (Twice Amended) A ferroelectric memory device comprising:

a ferroelectric capacitor including a top electrode, a bottom electrode and a ferroelectric film interposed between the top and bottom electrodes, the top electrode having a rectangular planar pattern;

a memory cell transistor including first and second doped layers and a gate, the memory cell transistor controlling a voltage supplied to the top electrode of the ferroelectric capacitor;

an interlevel dielectric film formed over the memory cell transistor and the ferroelectric capacitor;

a first interconnection layer formed on the interlevel dielectric film;

an upper interlevel dielectric film formed to cover the first interconnection layer; and

a second interconnection layer formed on the upper interlevel dielectric film,

wherein, in a planar layout of the ferroelectric memory device, the first interconnection layer partially overlaps with the top electrode of the ferroelectric capacitor, and does not cover at least one side of the rectangular top electrode, and the width of a bit line formed above the top electrode is smaller than the distance between the top electrode and another top electrode adjacent to the top electrode[; and

wherein the second interconnection layer totally covers the bottom electrode of the ferroelectric capacitor in the planar layout].